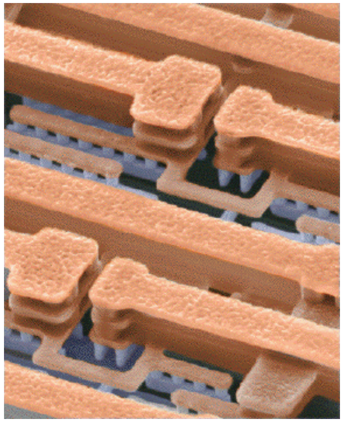
Tegal Cu/Low-k Dielectric Advanced Metallization Patent Portfolio

An opportunity to secure an Intellectual Property position in advanced copper and low-k dielectric technology



Prepared by:
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Chief Technologist
Tegal Corporation
February 2012

Executive Summary

Tegal's Cu/low-k Technology Patents were once part of a much larger portfolio of patents that spanned advanced applications in process and capital equipment encompassing a broad range of deposition, etch, photoresist strip, and integrated process technologies. Either as standalone portfolios, or with associated product lines, much of the portfolio has been placed into larger organizations that are much better positioned to benefit from the developed technologies.

The target audience for the Cu/low-k portfolio consists of IC manufacturers and IP aggregators that are seeking to expand their portfolio in the area of advanced metallization for IC devices. The portfolio is comprised of six patents that address a number of the issues associated with ongoing linewidth reductions in Cu/low-k metallization schemes.

Four of the six patents use controlled levels of oxygen to overcome adhesion issues that have been observed in atomic layer deposition of seed layers over barriers layers. ALD is seeing increased utilization particularly in the most advanced FLASH memory devices at the Metal1 layer. Additionally, one of the six patents describes an integrated process that provides for degassing of porous low-k dielectric layers prior to the deposition of a capping layer. This patent is highly relevant to the emergence and utilization of porous low-k dielectrics. One additional patent pertains to a multistep process that provides an integrated process for protection of process sensitive low-k dielectrics to ensure that the integrity of sidewalls are maintained prior to subsequent processing.

The patents in this portfolio are relevant to metallization schemes currently in production and are in areas of increasing interest for advanced metallization schemes.

Bids are currently being solicited for the Cu/low-k dielectric Technology patent portfolio and updates will be provided on the Tegal website (www.tegal.com) and through periodic press releases.

Tegal's Cu/low-k Patent Portfolio

US 6,495,449 Multilayered Diffusion Barrier Structure for Improving Adhesion Property

US 6,670,266 Multilayered Diffusion Barrier Structure for Improving Adhesion Property

US 6,777,331 Multilayered Copper Structure for Improving Adhesion Property

US 7,087,522 Multilayer Copper Structure for Improving Adhesion Property

US 6,919,101 Method to Deposit an Impermeable Film on Porous Low-k Dielectric Film

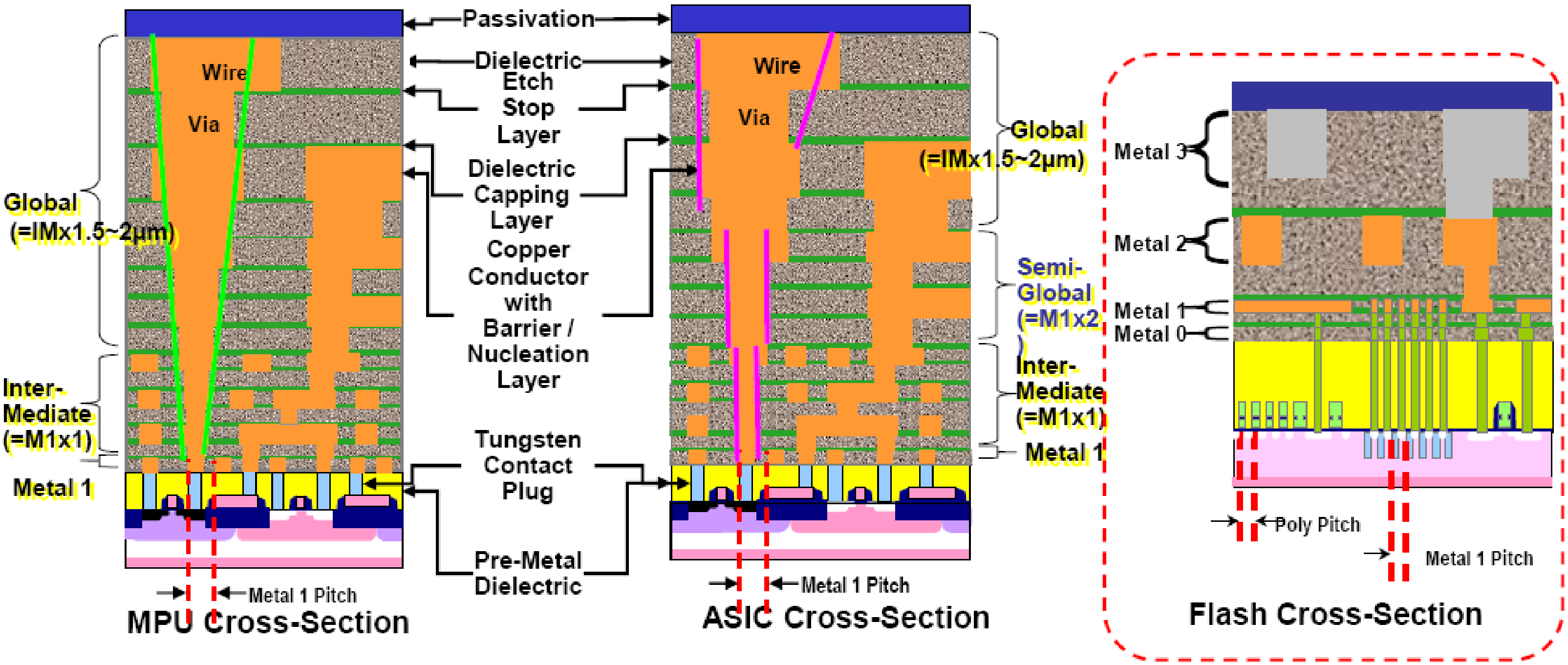
US 7,163,721 Method to Plasma Deposit on Organic Polymer Dielectric Film

General Challenges in ITRS Roadmap for Metallization

- Porous low-k dielectrics replacing bulk low-k dielectrics
- Complex Diffusion barrier + Seed layer structures
- Non-Cu seed layers for Cu fill
- Non-Cu fill at Metal1
- Increasing aspect ratio for progressively smaller devices particularly at Metal1

From Dec2011 ITRS Interconnect Winter Meeting:

Interconnect Technology Drivers



1) MPU: Revised hierarchy
2) ASIC: No drastic change, however semi-global should be kept at 2 x M1
3) Flash: The new technology driver for M1

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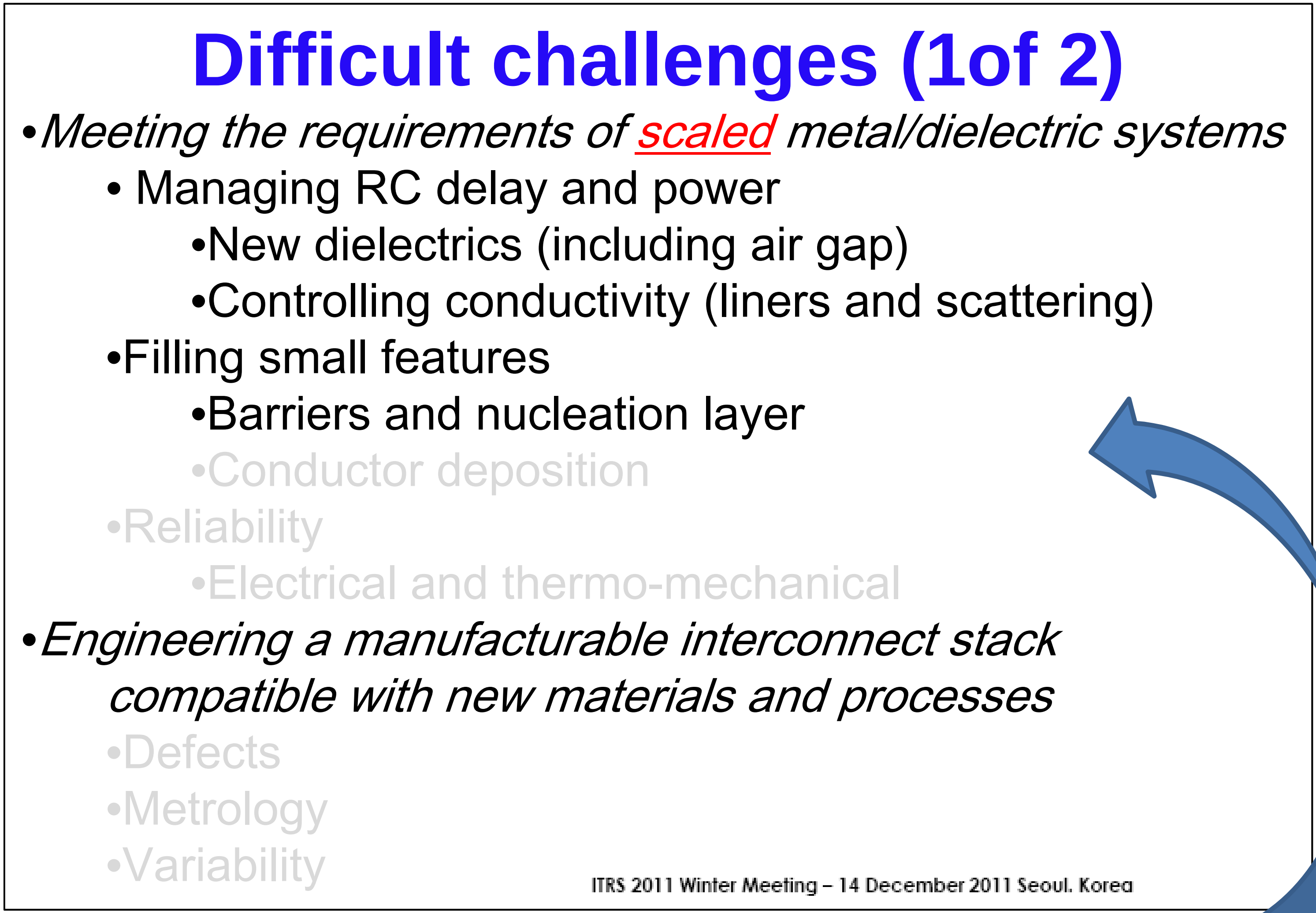
High aspect ratio structures increasingly employ ALD to deposit barriers and seed layers

From Dec2011 ITRS Interconnect Winter Meeting:



Difficult challenges (1of 2)

- *Meeting the requirements of scaled metal/dielectric systems*
  - Managing RC delay and power
    - New dielectrics (including air gap)
    - Controlling conductivity (liners and scattering)
  - Filling small features
    - Barriers and nucleation layer
    - Conductor deposition
  - Reliability
    - Electrical and thermo-mechanical
- *Engineering a manufacturable interconnect stack compatible with new materials and processes*
  - Defects
  - Metrology
  - Variability

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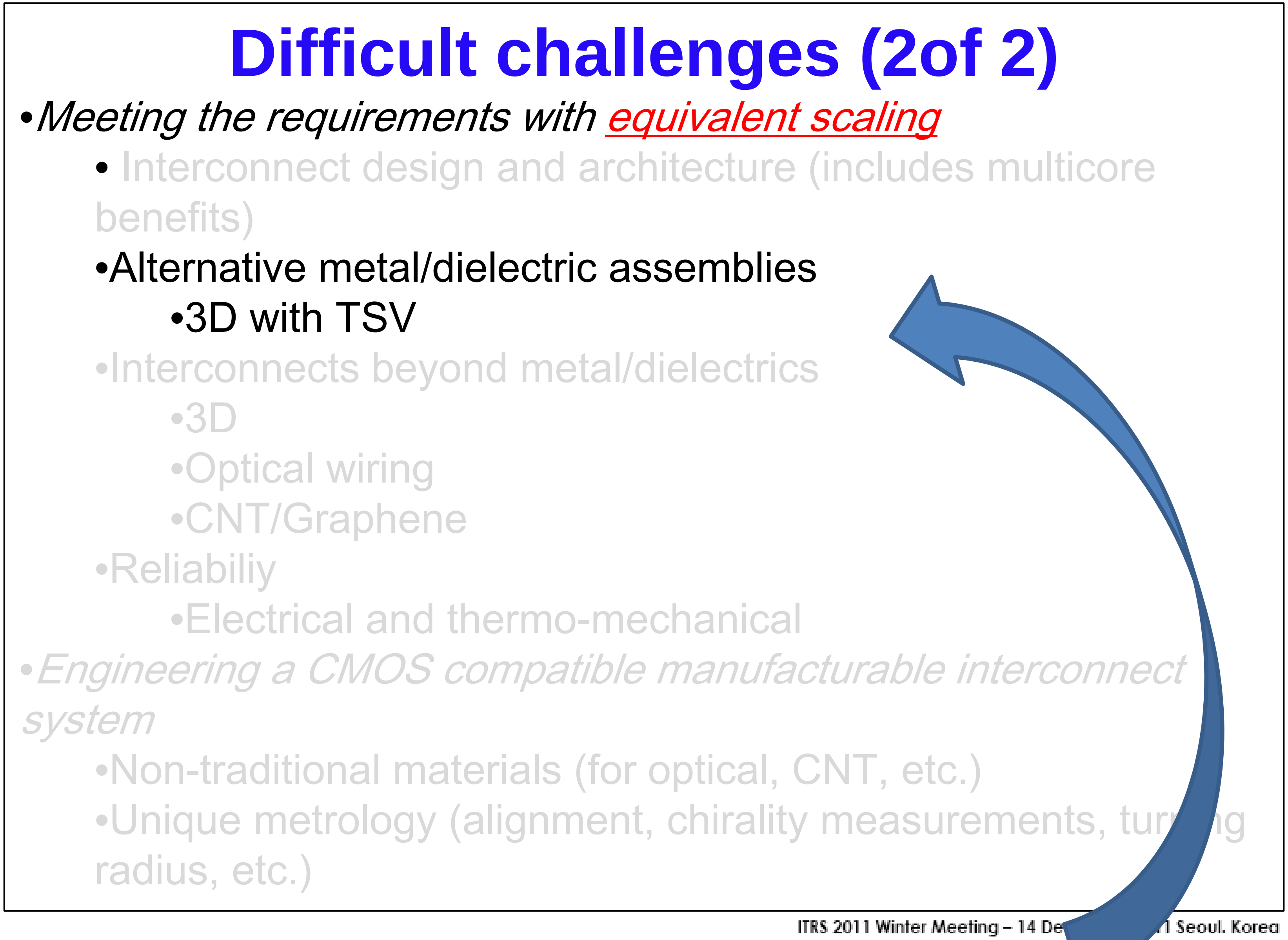
Tegal Patents are applicable to these development issues

From Dec2011 ITRS Interconnect Winter Meeting:



Difficult challenges (2of 2)

- *Meeting the requirements with equivalent scaling*
  - Interconnect design and architecture (includes multicore benefits)
  - Alternative metal/dielectric assemblies
    - 3D with TSV
  - Interconnects beyond metal/dielectrics
    - 3D
    - Optical wiring
    - CNT/Graphene
  - Reliabiliy
    - Electrical and thermo-mechanical
- *Engineering a CMOS compatible manufacturable interconnect system*
  - Non-traditional materials (for optical, CNT, etc.)
  - Unique metrology (alignment, chirality measurements, tur ng radius, etc.)

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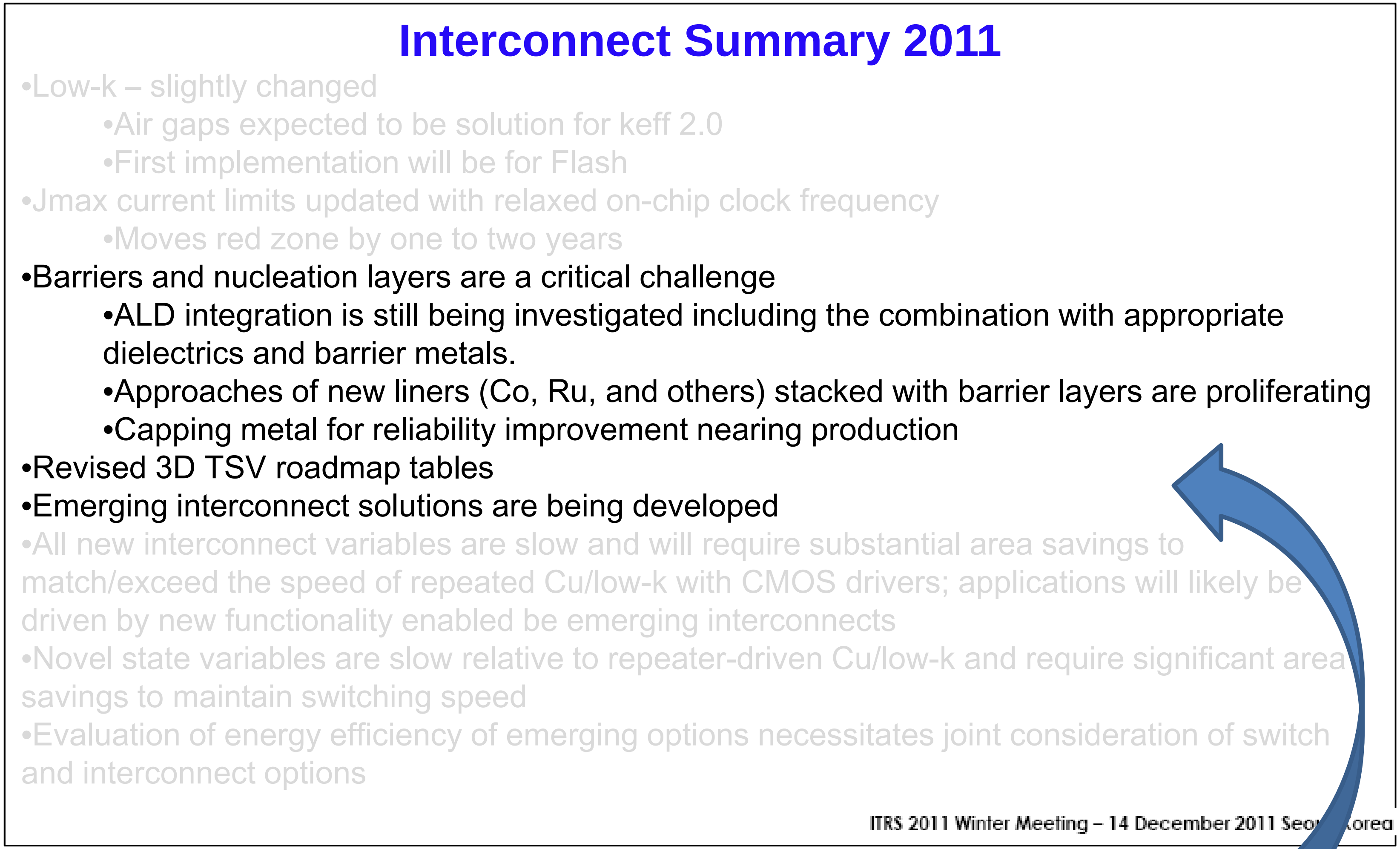
Tegal Patents are applicable to these development issues

From Dec2011 ITRS Interconnect Winter Meeting:



Interconnect Summary 2011

- Low-k – slightly changed
  - Air gaps expected to be solution for keff 2.0
  - First implementation will be for Flash
- Jmax current limits updated with relaxed on-chip clock frequency
  - Moves red zone by one to two years
- Barriers and nucleation layers are a critical challenge
  - ALD integration is still being investigated including the combination with appropriate dielectrics and barrier metals.
  - Approaches of new liners (Co, Ru, and others) stacked with barrier layers are proliferating
  - Capping metal for reliability improvement nearing production
- Revised 3D TSV roadmap tables
- Emerging interconnect solutions are being developed
- All new interconnect variables are slow and will require substantial area savings to match/exceed the speed of repeated Cu/low-k with CMOS drivers; applications will likely be driven by new functionality enabled be emerging interconnects
- Novel state variables are slow relative to repeater-driven Cu/low-k and require significant area savings to maintain switching speed
- Evaluation of energy efficiency of emerging options necessitates joint consideration of switch and interconnect options

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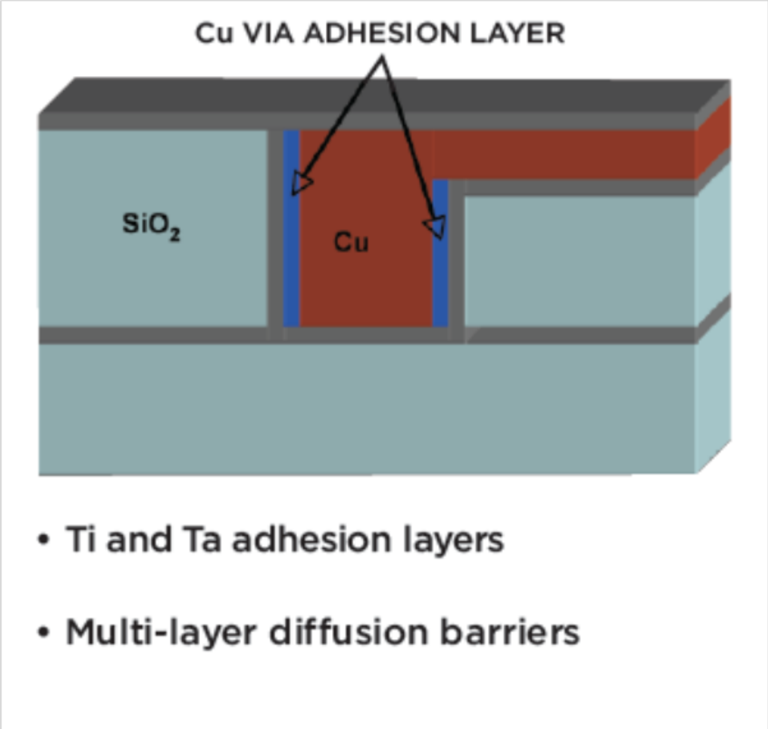
Tegal Patents are applicable to these development issues

Tegal Cu/low-k Technology patents

- Potential solution for Cu seed layer adhesion to barrier layers used in Cu metallization
- Potential solution for non-Cu seed layer adhesion to barrier layers used in Cu metallization
- Potential solution for Cu and non-Cu seed layer adhesion to barrier layers used in non-Cu metallization
- Integrated process for degassing and decontamination of porous low-k dielectrics before capping layer deposition
- Damage-free deposition on sensitive low-k polymer layers

Barrier and Adhesion Layer Technology



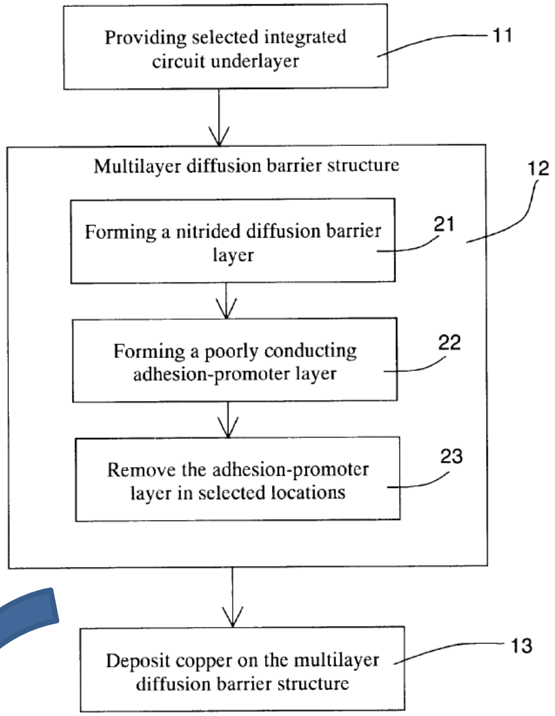
- Ti and Ta adhesion layers
- Multi-layer diffusion barriers

<u>US Patents</u>

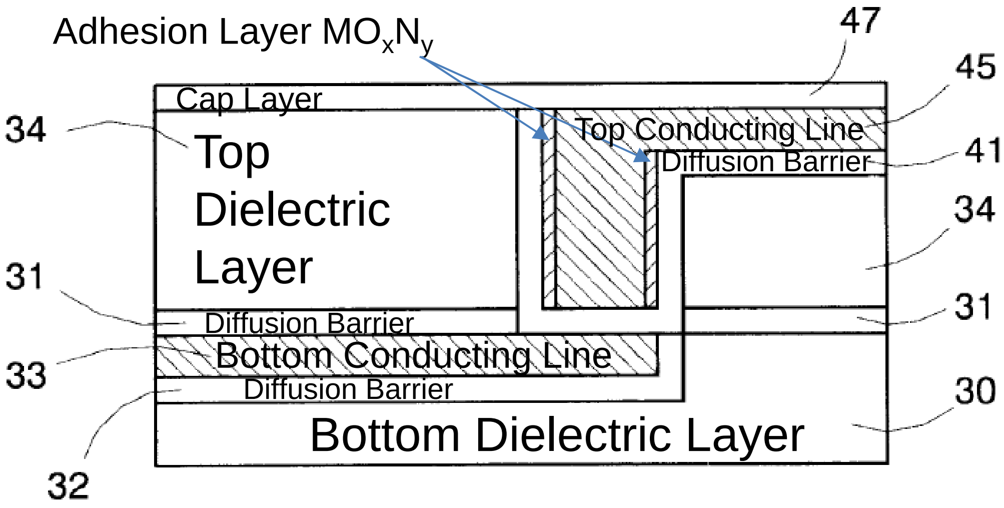
6,495,449
6,777,331
6,670,266
7,087,522

Four patents pertaining to the strategic oxygen incorporation into barrier layers and seed layers, sometimes in minute quantities, to improve the adhesion between metal fill (typically Cu) and underlying barrier layers (typically Ti & Ta-based layers)

Multilayer **Diffusion Barrier** Structure - Patent US#6,670,266



Typical Diffusion Barriers:
TiN, TiSiN, TaN, TaSiN, WN, WSiN



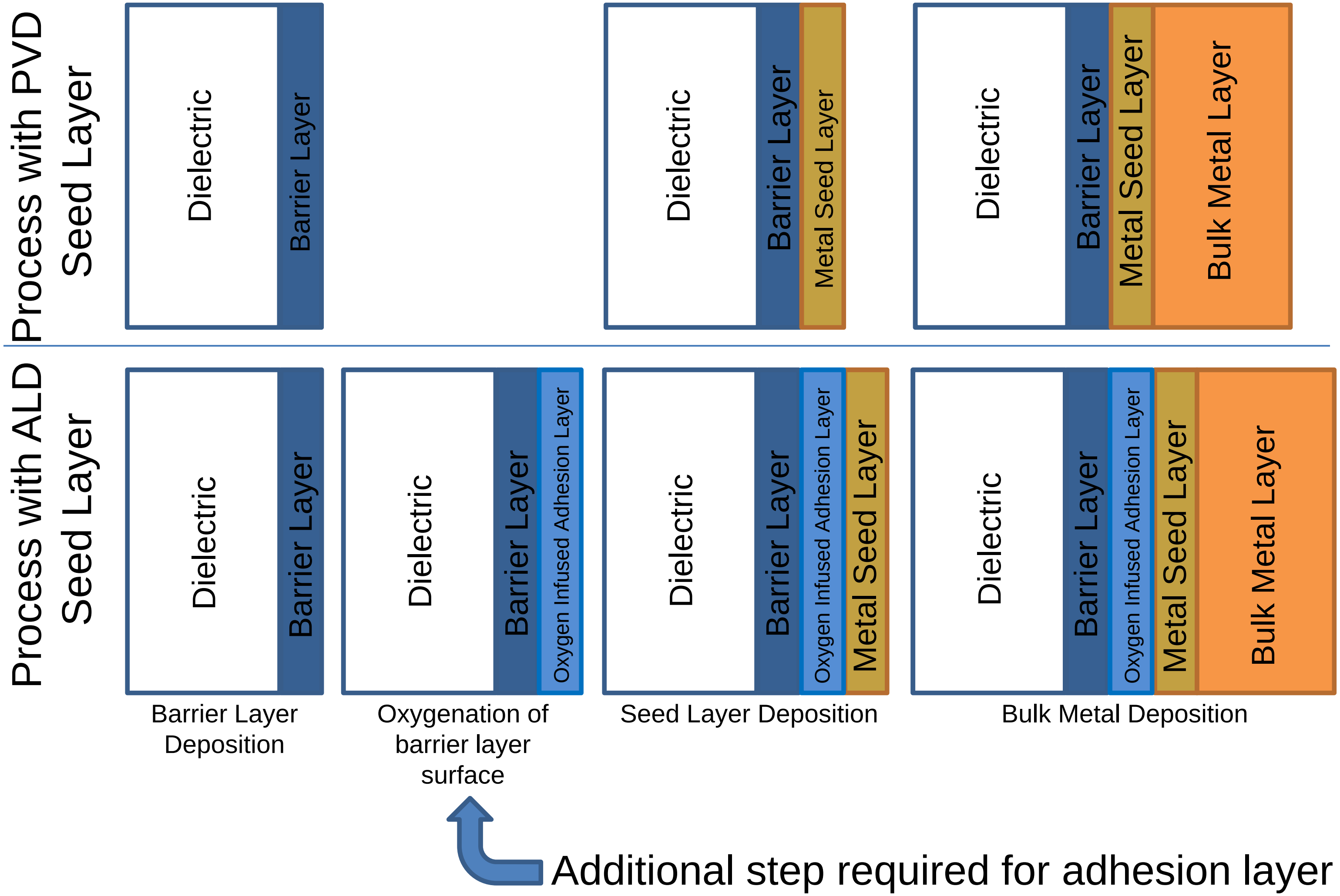
Summary:

Method for forming a Metal oxy-nitride (MO_xN_y) layer over a Metal Nitride diffusion barrier to improve adhesion on the sidewalls of via structures (Ta, Ti, & W typical)

Of particular importance in high aspect ratio structures

Applicable to wide range of conducting line materials: Cu, W, Si, etc.

Comparison of Conventional PVD Seed Layer Process Sequence with Advanced ALD Seed Layer Process Sequence



Barrier Layer Deposition

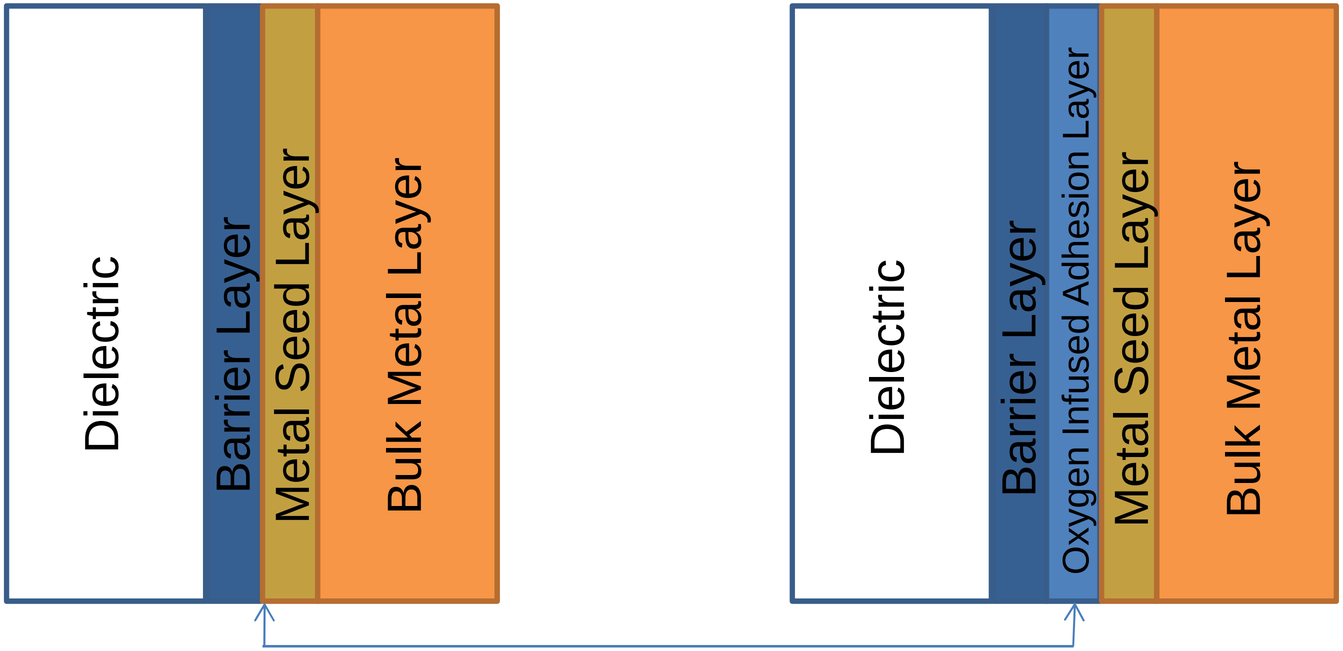
Oxygenation of barrier layer surface

Seed Layer Deposition

Bulk Metal Deposition

Additional step required for adhesion layer

Comparative Detail of Barrier/Adhesion/Seed/Bulk Metal Layers deposited by PVD and ALD

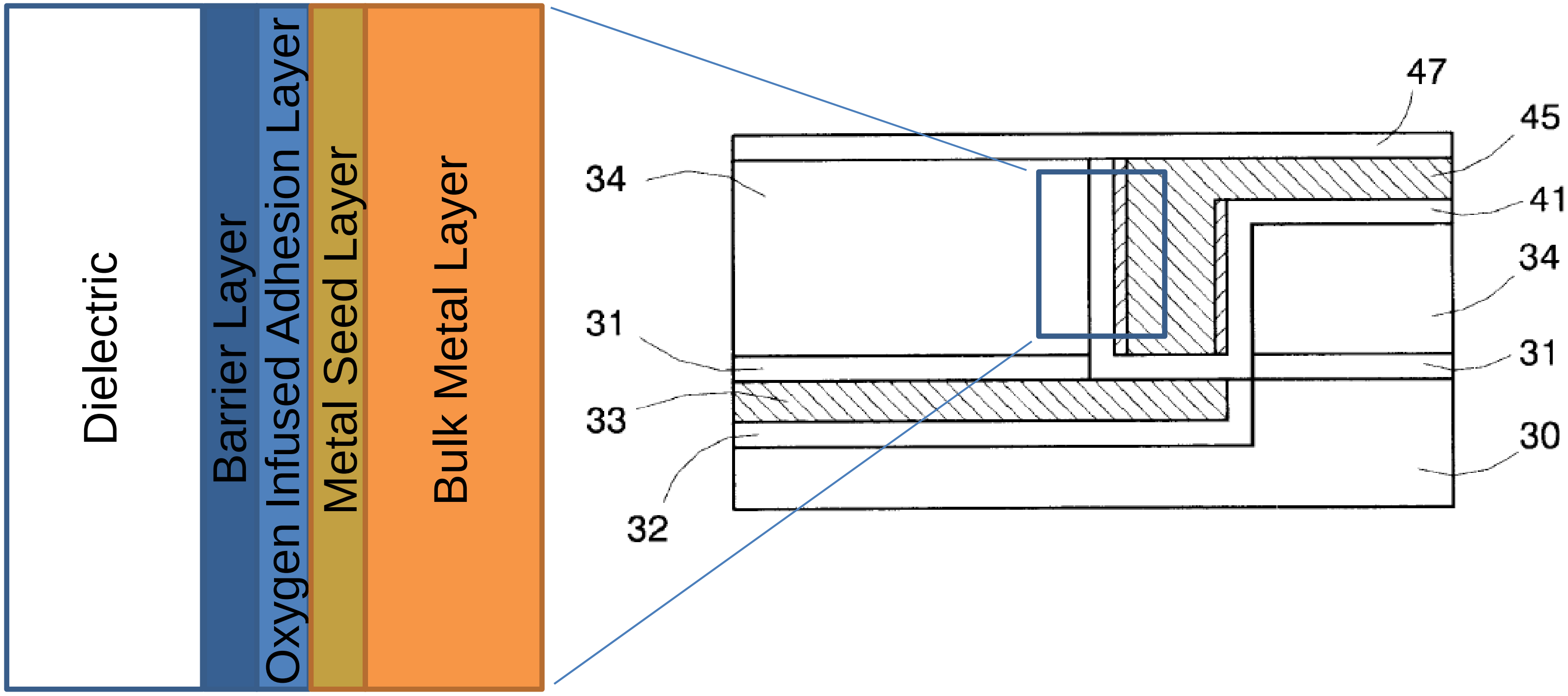


Conventional Seed Layer deposition w/PVD does not require special adhesion layer to barrier layer

In high aspect ratio applications that employ ALD, adhesion layer is used to bond copper seed to underlying barrier layer

ALD is seeing increasing implementation in high aspect ratio metallization structures for which PVD is not well suited

Detail of Barrier/Adhesion/Seed/Bulk Metal Layers Deposition with ALD Seed Layer



Dielectric

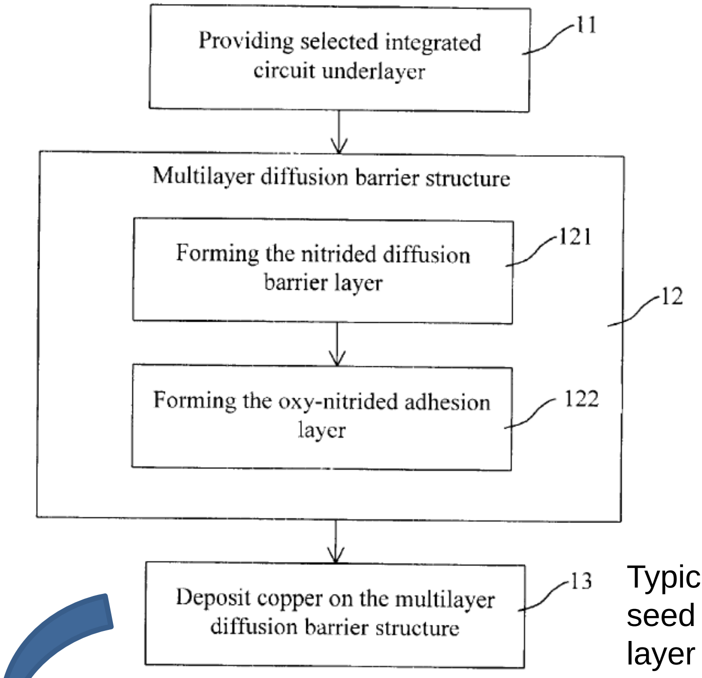
Barrier Layer

Oxygen Infused Adhesion Layer

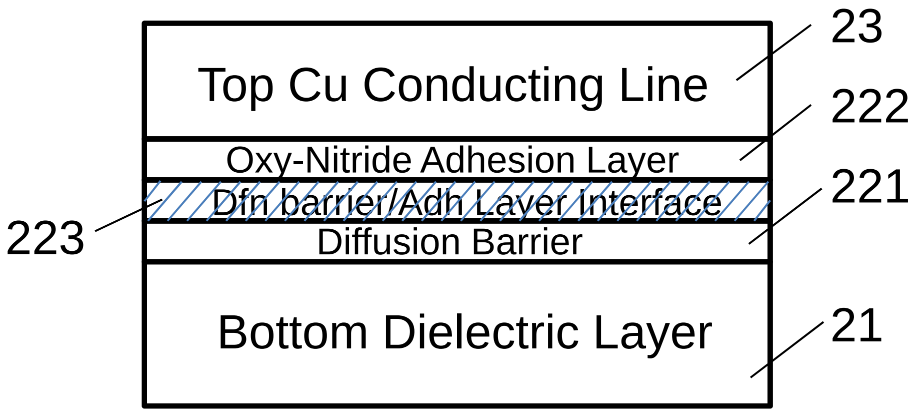
Metal Seed Layer

Bulk Metal Layer

Multilayer **Diffusion Barrier** Structure - Patent US#6,495,449



Typical seed layer



Typical Diffusion Barriers:
TiN, TiSiN, TaN, TaSiN, WN, WSiN

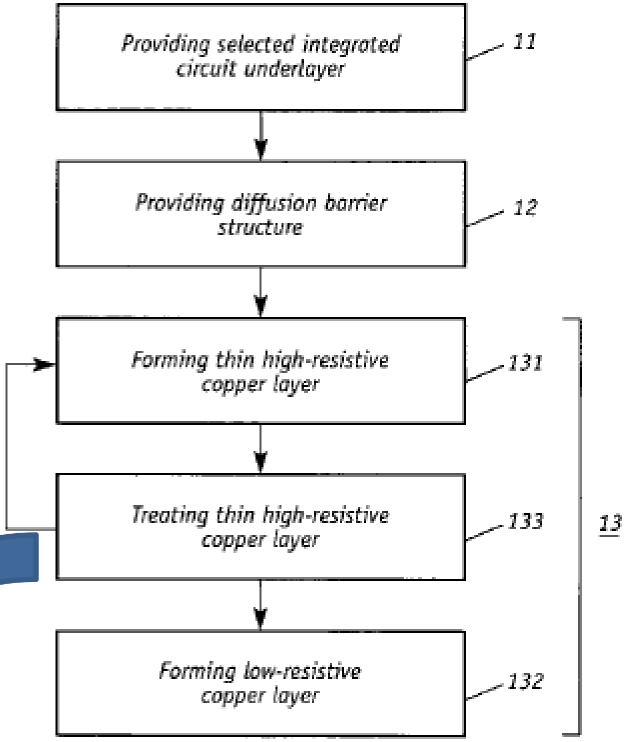
Summary:

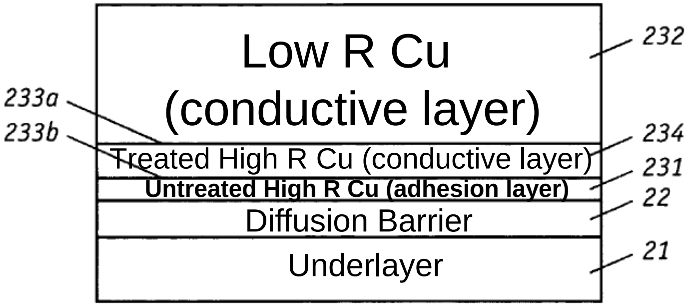
Method for forming a Metal oxy-nitride (MO_xN_y) layer over a Metal Nitride diffusion barrier to improve adhesion of subsequently deposited conductor layers (Ta, Ti, & W typical)

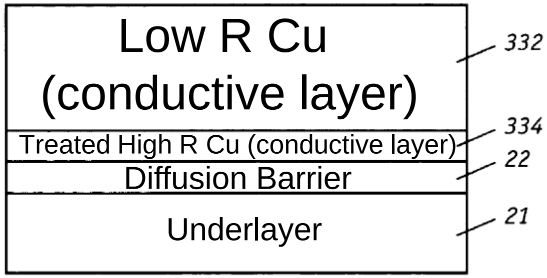
Of particular importance in high aspect ratio structures

Applicable to wide range of conducting line materials: Cu, W, Si, etc.

Cu **Adhesion** Layer
Patent US#6,777,449







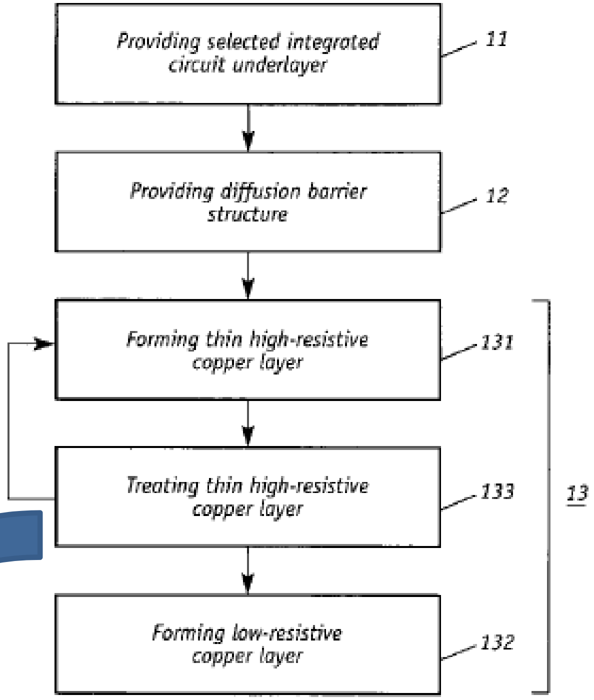
231 adhesion layer consumed

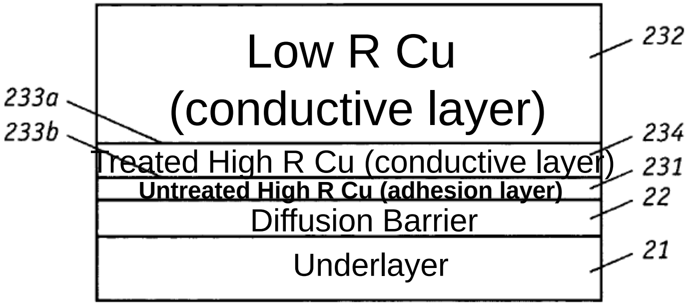
Summary: Method for forming a copper seed/adhesion layer over a diffusion barrier to secure a copper post;

Of particular importance in high aspect ratio structures in which the seed/adhesion layers must be deposited with ALD

Relevant to copper seed/adhesion layers

Metal Film **Adhesion** Layer
Patent US#7,087,522



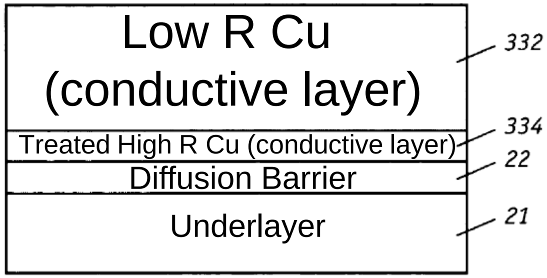

Low R Cu (conductive layer)

Treated High R Cu (conductive layer)

Untreated High R Cu (adhesion layer)

Diffusion Barrier

Underlayer


Low R Cu (conductive layer)

Treated High R Cu (conductive layer)

Diffusion Barrier

Underlayer

231 adhesion layer consumed

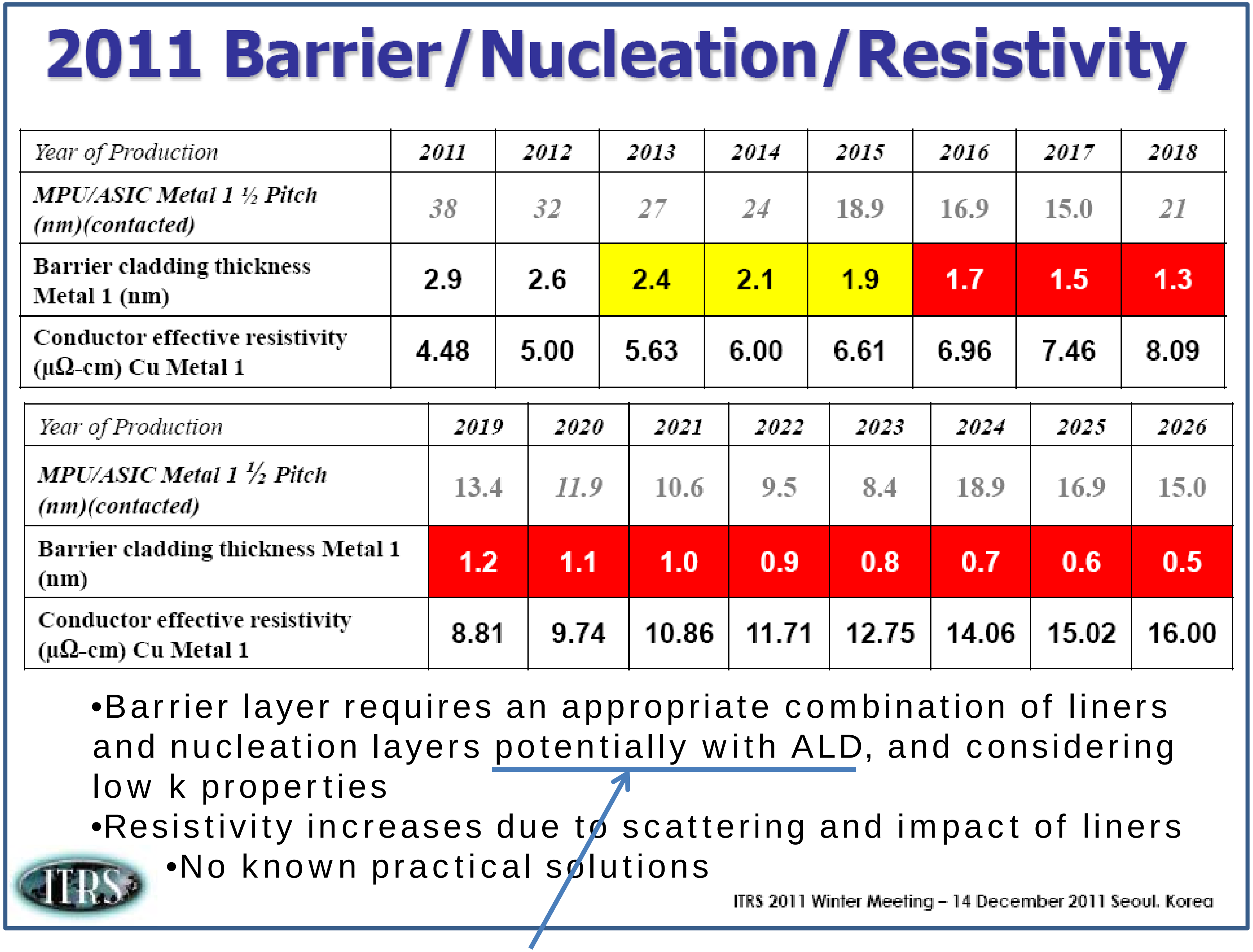
Summary:

Method for forming a copper seed/adhesion layer , comprised of a metal, over a diffusion barrier to secure a copper post;

Of particular importance in high aspect ratio structures in which the seed/adhesion layers must be deposited with ALD

Relevant to Ru, Mo, and other non-Cu adhesion/seed layer options

From Dec2011 ITRS Interconnect Winter Meeting:



2011 Barrier/Nucleation/Resistivity

Year of Production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	38	32	27	24	18.9	16.9	15.0	21
Barrier cladding thickness Metal 1 (nm)	2.9	2.6	2.4	2.1	1.9	1.7	1.5	1.3
Conductor effective resistivity (µΩ-cm) Cu Metal 1	4.48	5.00	5.63	6.00	6.61	6.96	7.46	8.09

Year of Production	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	13.4	11.9	10.6	9.5	8.4	18.9	16.9	15.0
Barrier cladding thickness Metal 1 (nm)	1.2	1.1	1.0	0.9	0.8	0.7	0.6	0.5
Conductor effective resistivity (µΩ-cm) Cu Metal 1	8.81	9.74	10.86	11.71	12.75	14.06	15.02	16.00

- Barrier layer requires an appropriate combination of liners and nucleation layers potentially with ALD, and considering low k properties
- Resistivity increases due to scattering and impact of liners
  - No known practical solutions

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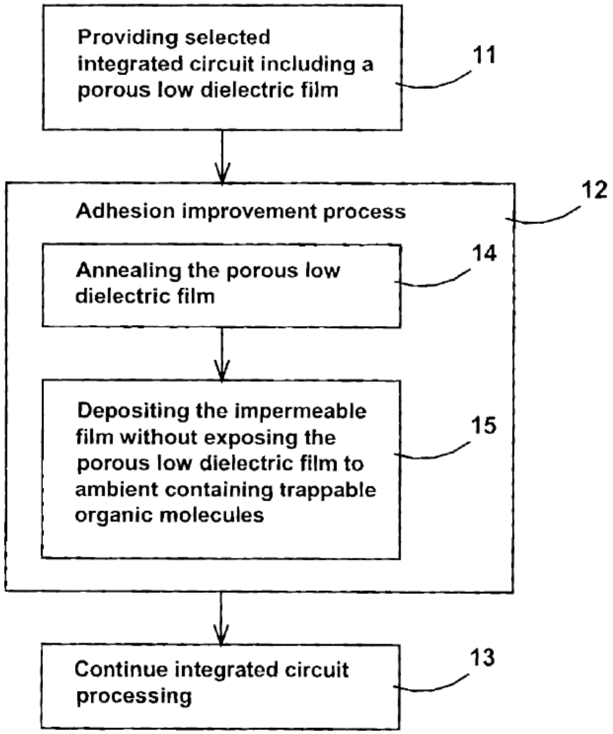
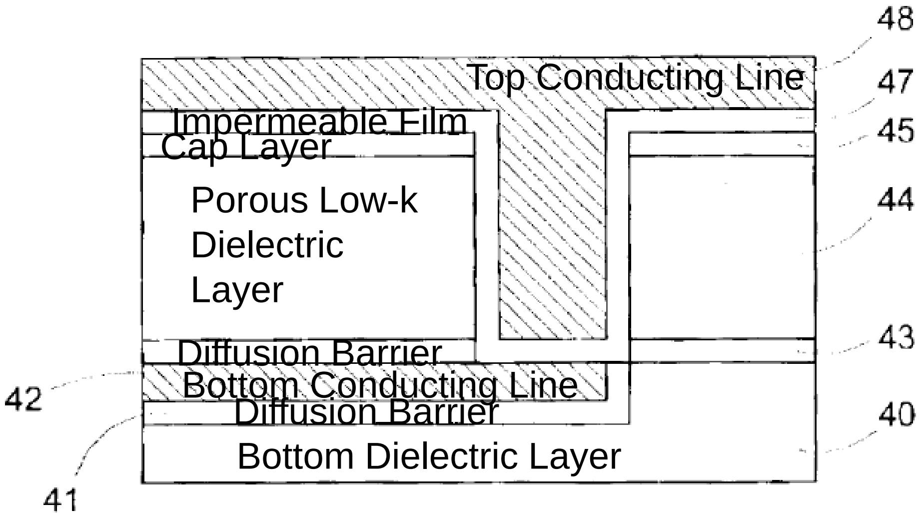
Tegal Patents are applicable to improving ALD seed layer adhesion

Impermeable Film Deposition on Porous low-k Dielectric - Patent US#6,919,101

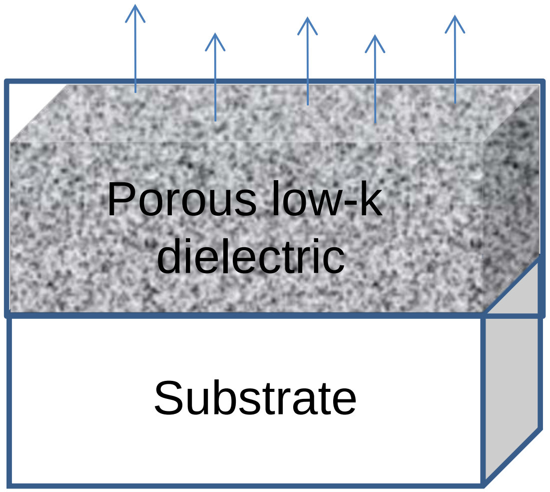


In-situ annealing/pore-evacuation step prior to depositing the impermeable cap layer



Typical Impermeable Films: TiN, TiSiN, TaN, TaSiN, WN, WSiN, SiO_2, Si_xN_y

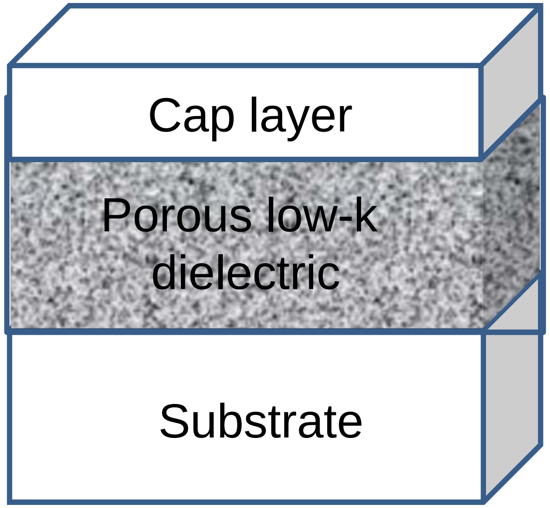
Impermeable Film Deposition on Porous low-k Dielectric - Patent US#6,919,101



Porous low-k dielectric

Substrate

Degas Anneal



Cap layer

Porous low-k dielectric

Substrate

In situ Cap layer deposition after Anneal

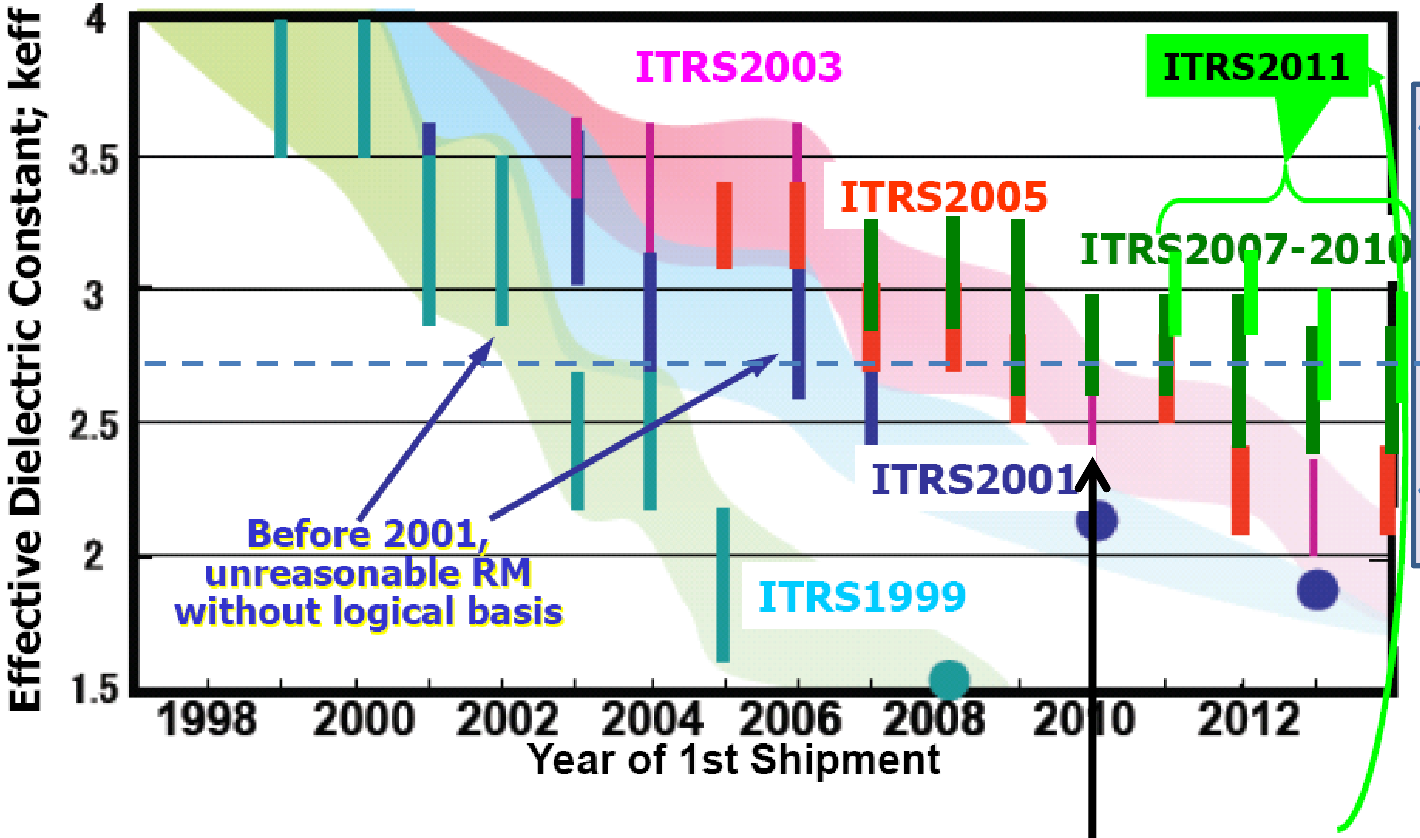
Integrated Porous low-k Degas and *in-situ* Capping Layer Deposition Process

Applicable to structures utilizing porous low-k dielectric layers ; effective evacuation of pores can significantly improve adhesion

Ref: See, for example, Liu, et al, JVST B25(3), May/June 2007, 906-912
and Fayolle, et al, Microelectronic Engineering 70 (2003) 255-266

From Dec2011 ITRS Interconnect Winter Meeting:

Historical Transition of ITRS Low-κ Roadmap



Bulk
Low-k
k>2.7

Porous
Low-k
k>2.7

Narrowed effective range due to elimination of hybrid stack

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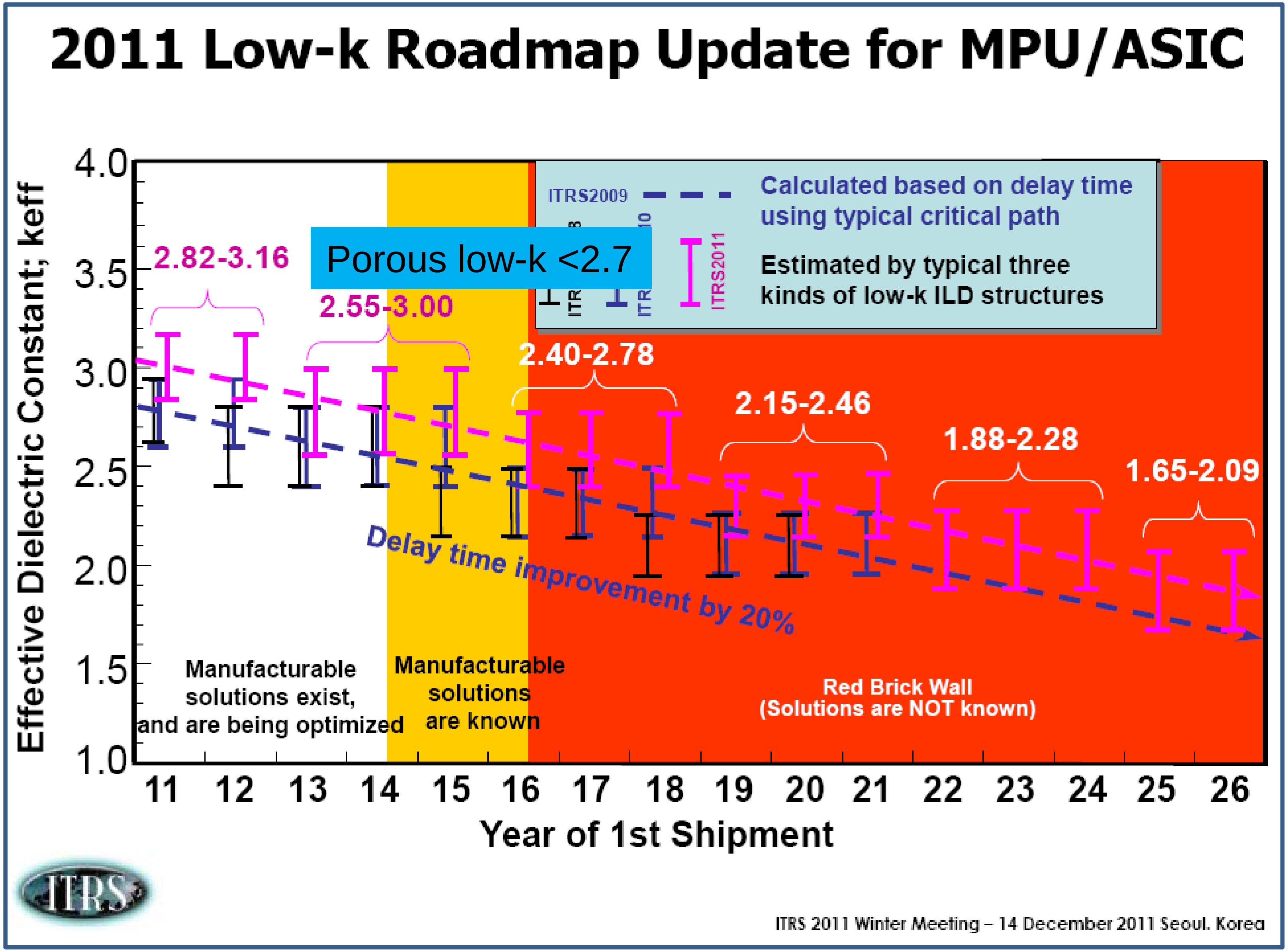
Transition to k<2.7

From Dec2011 ITRS Interconnect Winter Meeting:



2011 Low-k Roadmap Update for MPU/ASIC

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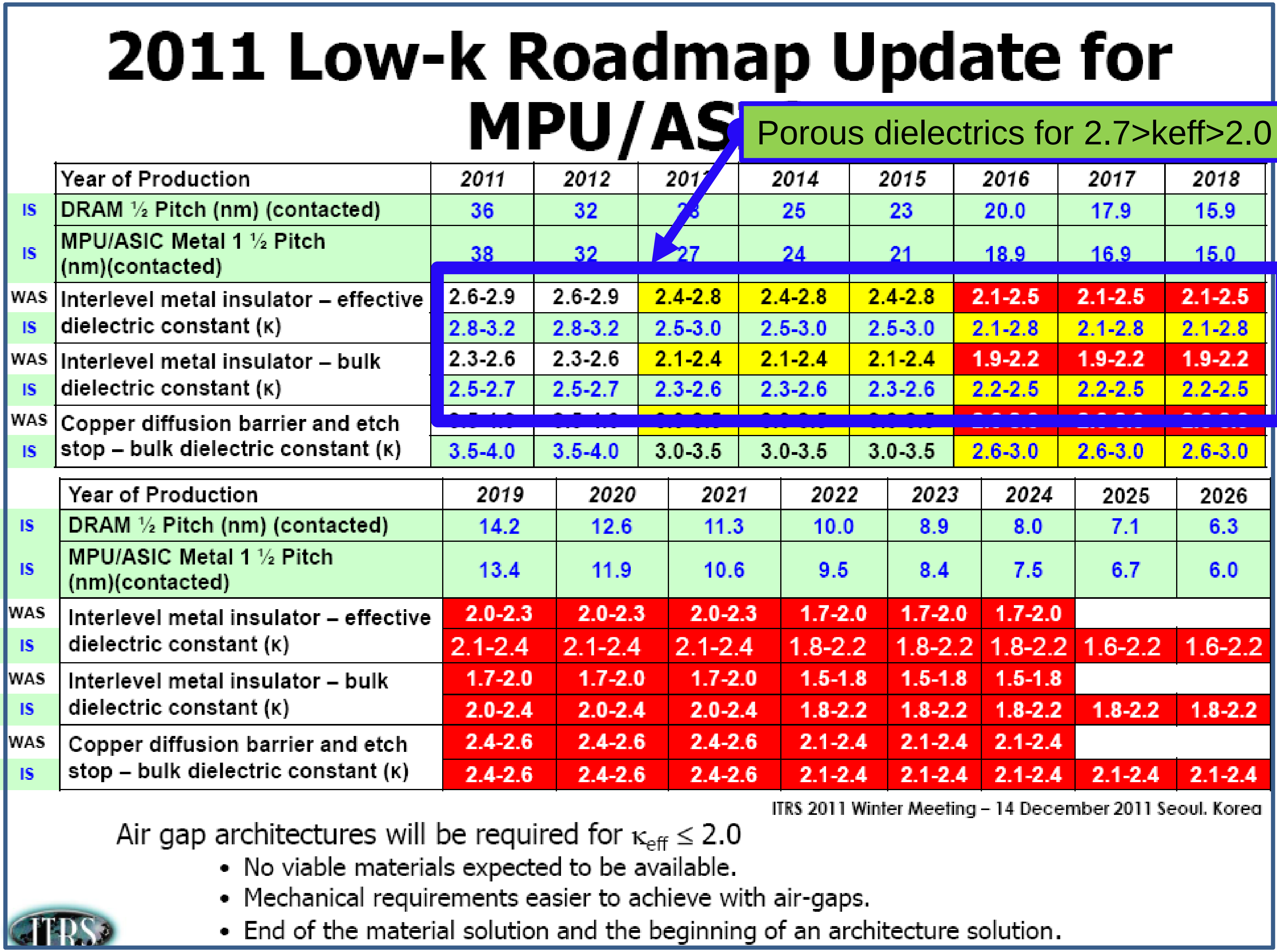
From Dec2011 ITRS Interconnect Winter Meeting:



2011 Low-k Roadmap Update for MPU/AS

Porous dielectrics for 2.7>keff>2.0

	Year of Production	2011	2012	2013	2014	2015	2016	2017	2018
IS	DRAM ½ Pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9
IS	MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	38	32	27	24	21	18.9	16.9	15.0
WAS	Interlevel metal insulator – effective dielectric constant (κ)	2.6-2.9	2.6-2.9	2.4-2.8	2.4-2.8	2.4-2.8	2.1-2.5	2.1-2.5	2.1-2.5
IS		2.8-3.2	2.8-3.2	2.5-3.0	2.5-3.0	2.5-3.0	2.1-2.8	2.1-2.8	2.1-2.8
WAS	Interlevel metal insulator – bulk dielectric constant (κ)	2.3-2.6	2.3-2.6	2.1-2.4	2.1-2.4	2.1-2.4	1.9-2.2	1.9-2.2	1.9-2.2
IS		2.5-2.7	2.5-2.7	2.3-2.6	2.3-2.6	2.3-2.6	2.2-2.5	2.2-2.5	2.2-2.5
WAS	Copper diffusion barrier and etch stop – bulk dielectric constant (κ)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
IS		3.5-4.0	3.5-4.0	3.0-3.5	3.0-3.5	3.0-3.5	2.6-3.0	2.6-3.0	2.6-3.0

	Year of Production	2019	2020	2021	2022	2023	2024	2025	2026
IS	DRAM ½ Pitch (nm) (contacted)	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
IS	MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	13.4	11.9	10.6	9.5	8.4	7.5	6.7	6.0
WAS	Interlevel metal insulator – effective dielectric constant (κ)	2.0-2.3	2.0-2.3	2.0-2.3	1.7-2.0	1.7-2.0	1.7-2.0		
IS		2.1-2.4	2.1-2.4	2.1-2.4	1.8-2.2	1.8-2.2	1.8-2.2	1.6-2.2	1.6-2.2
WAS	Interlevel metal insulator – bulk dielectric constant (κ)	1.7-2.0	1.7-2.0	1.7-2.0	1.5-1.8	1.5-1.8	1.5-1.8		
IS		2.0-2.4	2.0-2.4	2.0-2.4	1.8-2.2	1.8-2.2	1.8-2.2	1.8-2.2	1.8-2.2
WAS	Copper diffusion barrier and etch stop – bulk dielectric constant (κ)	2.4-2.6	2.4-2.6	2.4-2.6	2.1-2.4	2.1-2.4	2.1-2.4		
IS		2.4-2.6	2.4-2.6	2.4-2.6	2.1-2.4	2.1-2.4	2.1-2.4	2.1-2.4	2.1-2.4

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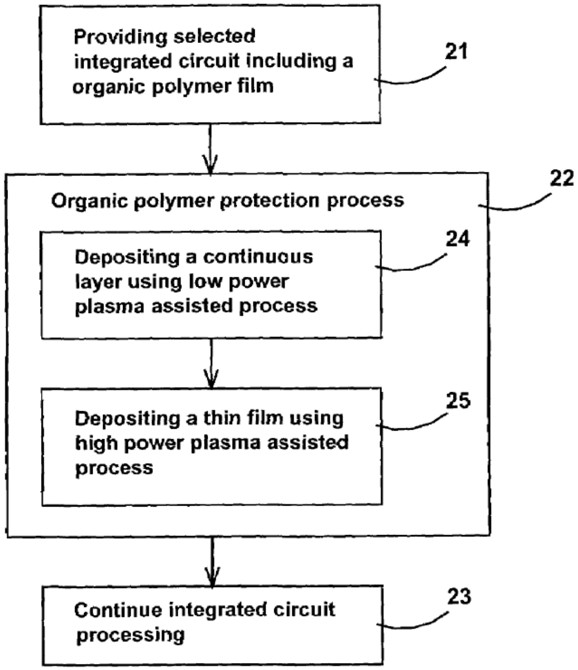
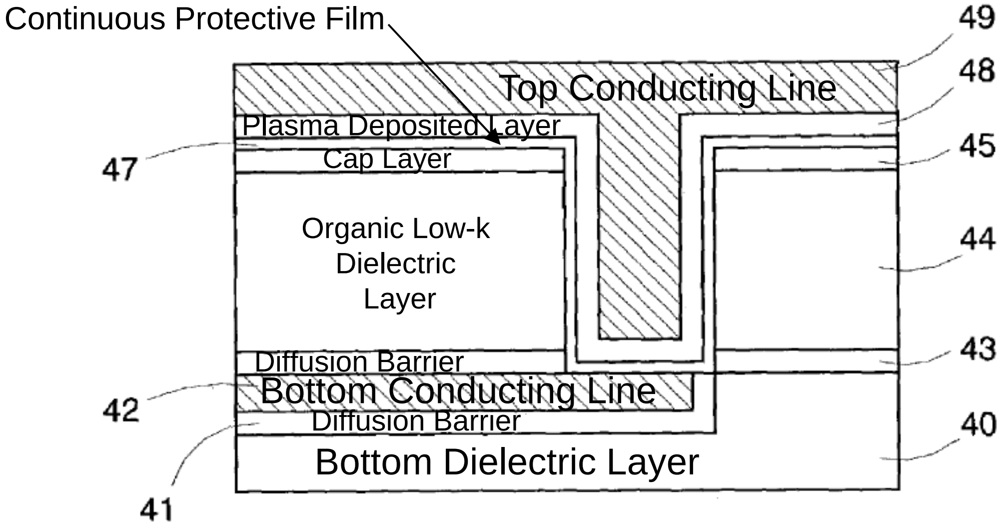
Air gap architectures will be required for $\kappa_{eff} \leq 2.0$

- No viable materials expected to be available.
- Mechanical requirements easier to achieve with air-gaps.
- End of the material solution and the beginning of an architecture solution.

Film Deposition on Organic Polymer Dielectric - Patent US#7,163,721



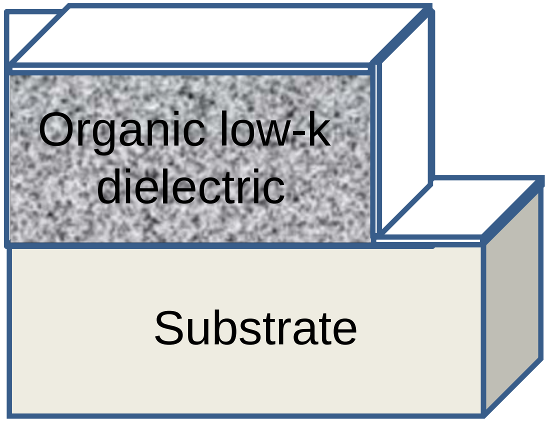


Summary:
Low or no power first deposition step preceding a standard deposition step

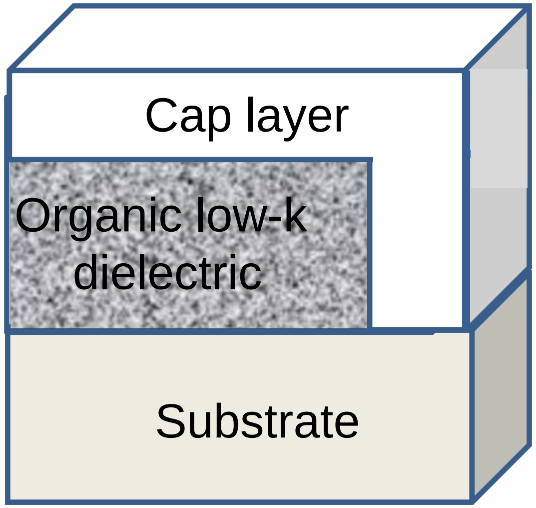
Typical continuous protective films are TiN and SiO_2

Typical Deposition Modules are PEALD, PECVD, PENLD

Film Deposition on Organic Polymer Dielectric - Patent US#7,163,721

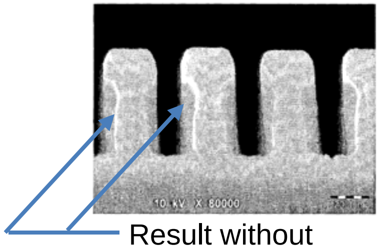


Low or no power first deposition step for cap or sealing layer



Higher power second deposition step for cap or sealing layer

Soft deposition step for damage sensitive, organic dielectric films



Result without initial low power step

Applicable to structures and processes for which organic dielectric layers are utilized

Summary

- The ITRS roadmap includes ongoing implementation of porous low-k dielectrics and suggests an eventual displacement of PVD-based barrier and seed layers with ALD-based layers starting with Flash at Metal1
- Tegal’s Cu/low-k patent portfolio provides an opportunity to obtain patents in the integration of porous low-k dielectrics and ALD-based adhesion layers